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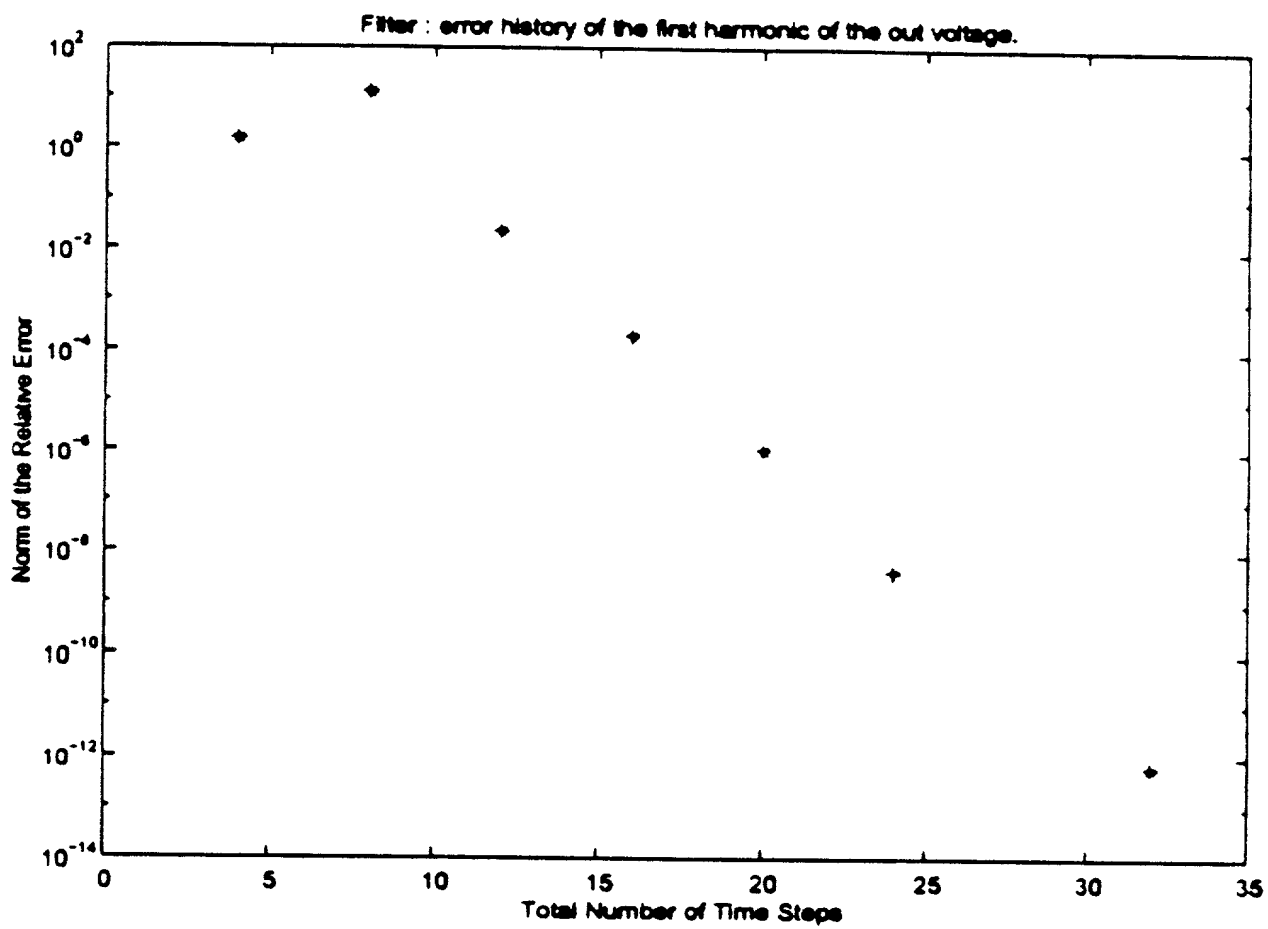


FIG. 1

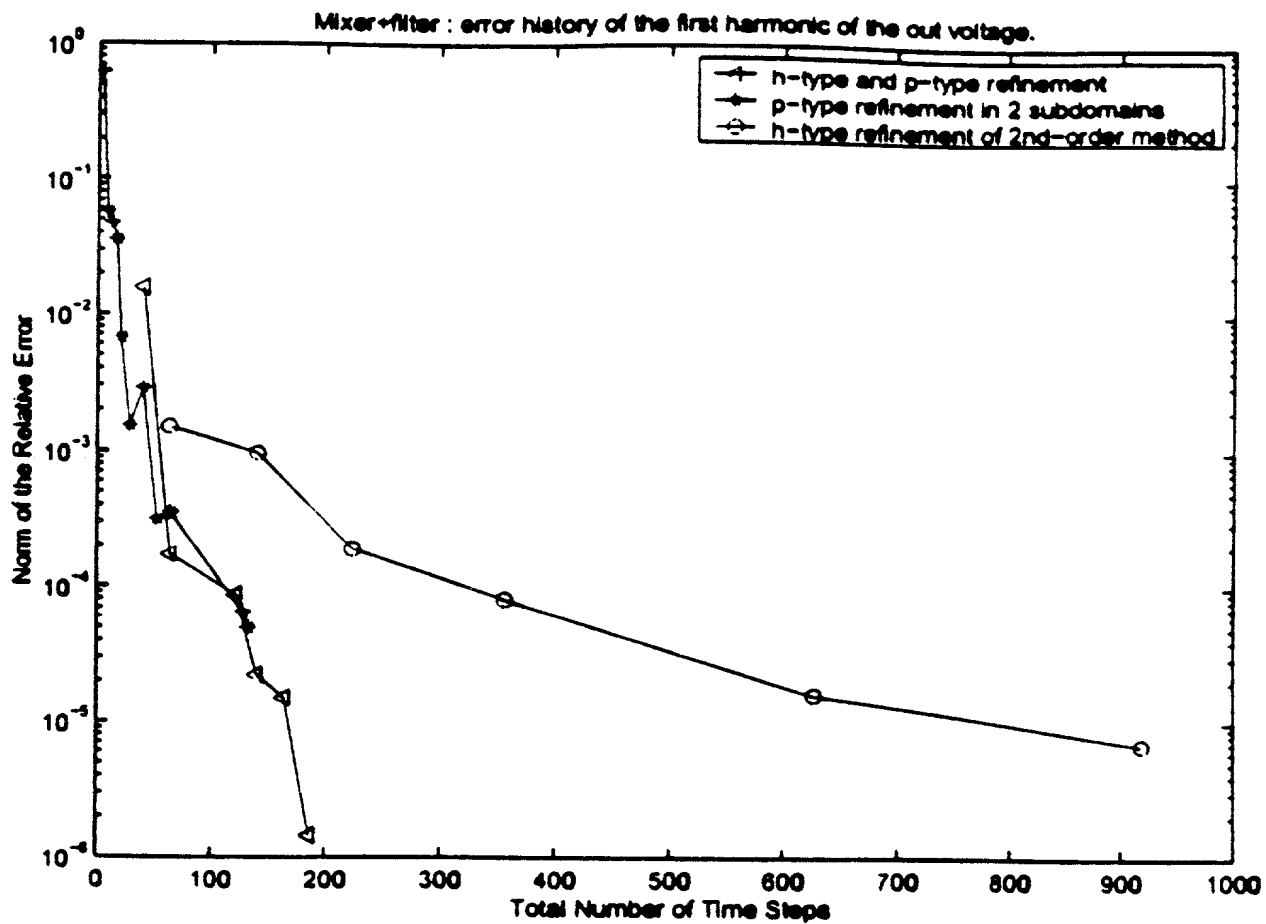


FIG. 2

Figure 10 is a line plot titled "DC-DC converter : nmos source voltage." showing the number of nodes (N) on the y-axis (ranging from -2 to 10) versus Time (second) on the x-axis (ranging from 0 to 1, scaled by 10^{-6}). The plot compares two refinement strategies:

- p-type refinement in 2 subdomains** (represented by 'x' markers)
- h-type and p-type refinement** (represented by '+' markers)

Both strategies show a sharp increase in the number of nodes around 0.3×10^{-6} seconds, peaking at approximately 9 nodes, and then decreasing back to near zero by 1.0×10^{-6} seconds. The h-type and p-type refinement strategy generally maintains a slightly higher number of nodes during the peak compared to the p-type refinement in 2 subdomains strategy.

FIG. 3